Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1. (Cancelled).

Claim 2. (Currently Amended) A process for producing a semiconductor wafer with a front surface and a back surface and an epitaxial layer of semiconducting material deposited on the front surface, wherein the process comprises the following process steps:

a) a stock removal polishing step as the only polishing step:

b) cleaning and drying of the semiconductor wafer;

c) pretreating of the front surface of the semiconductor wafer in a first step in a hydrogen atmosphere at a temperature of 950°C to 1250°C to remove oxide from the front surface of the wafer, and then, in a second step, with ~~to which gaseous Hcl has been admixed~~ a mixture of hydrogen and HCl at a temperature of from 950°C to 1250°C ~~degrees Celsius in an epitaxy reactor~~, ~~thereby removing~~ to selectively etch said front surface and remove from 0.01 to 0.2 μm of material from the front surface of the semiconductor wafer at an etching rate of 0.01 to 0.1 μm/min; and

d) depositing ~~of the~~ an epitaxial layer on the front surface of the pretreated semiconductor wafer.

Claim 3. (Currently Amended) The process ~~as claimed in~~ of claim 2, comprising

polishing the front surface and the back surface of the semiconductor wafer simultaneously during the stock removal polishing.

Claim 4. (Currently Amended) The process ~~as claimed in~~ of claim 2, comprising

polishing only the front surface of the semiconductor wafer during the stock removal polishing.

Claim 5. (Currently Amended) The process as claimed in claim 2, comprising

carrying out the pretreating referred to in step (c) immediately before ~~the epitaxial~~ depositing the epitaxial layer ~~in the epitaxy reactor~~.

Claim 6. (Currently Amended) The process ~~as claimed in~~ of claim 2, comprising

treating the semiconductor wafer, in a first step of the pretreating according to step (c), in a hydrogen atmosphere at a temperature of from ~~950~~ 1100 to ~~1250~~ 1150 degrees Celsius.

Claim 7. (Cancelled)

Claim 8. (Currently Amended) The process ~~as claimed in~~ of claim 2,

wherein the epitaxial layer deposited in step (d) has a thickness of 0.3 μm to 10 μm and is deposited at a temperature of from 600°C to 1250°C.

Claim 9. (Currently Amended) The process ~~as claimed in~~ of claim 2,

wherein the epitaxial layer deposited in step (d) is rendered hydrophilic using an oxidizing gas.

Claim 10. (Currently Amended) The process ~~as claimed in~~ of claim 2,

wherein the epitaxial layer deposited in step (d) is rendered hydrophilic by wet-chemical means.

Claim 11. (Original) In a method for producing integrated semiconductor components, the improvement which comprises

utilizing an epitaxially coated semiconductor wafer produced by the process of claim 2 for producing said components.

Claim 12. (New) A process for preparation of an epitaxially coated silicon wafer having a front surface and a back surface, comprising

a) polishing at least the front surface of a silicon wafer in a single removal polishing step to produce a polished silicon wafer having a polished front surface with a surface roughness of 0.05 to 0.29 nm RMS over 1 μm x 1 μm;

b) cleaning and drying the polished silicon wafer;

c) thermally treating the polished silicon wafer by

c)i) in a first step, removing native oxide by treating with H_2 at a temperature of 950°C to 1200°C; and

c)ii) subsequently etching the polished silicon wafer in a mixture of H_2 and gaseous HCl at a temperature of from 1100°C to 1180°C to remove 0.01 to 0.2 μm of silicon from said front surface, the concentration of HCl such that the etch rate is from 0.01 to 0.1 μm/min; and

d) depositing an epitaxial layer onto said front surface.

13. (New) The process of claim 12, wherein step c)i) is performed at a temperature of 1100°C to 1150°C.

14. (New) The process of claim 12, wherein said silicon wafer is a boron-doped silicon wafer.

15. (New) The process of claim 12, wherein said silicon wafer is an n-type silicon wafer doped with at least one of phosphorus, arsenic, or antimony.